REMARKS

In response to the Official Action mailed July 7, 2003, Applicant amends his application and requests reconsideration. Claim 16 is cancelled and claims 19 and 20 are added, so that claims 1-15, and 17-20 are now pending.

Claims 1-4, 10-15, 17, and 18 were allowed. In this Amendment, a clarifying, non-substantive change is made in claim 3 identifying the capacitor more clearly, and claim 8 is correspondingly amended for clarity. Nearly all claims are amended for clarity with respect to the term "metallic layer". The shielding layers clearly must include a metal to be effective in electromagnetic shielding and that description is retained in amended claims 1, 10, and 14. Likewise, the capacitor electrode must include a metal, and that description is retained in amended claims 3, 8, 12, and 17. Further, the bit line layer must include a metal and that description is preserved in amended claims 2, 7, and 11. It is not essential that the gate electrode layer be a metal, so the reference to metallic layers in claims 6 and 15 is modified. The patent application points out, for example at page 9, lines 14-23, that the gate electrode of the transistors in the claimed structure may include a polysilicon film as well as a silicide layer and, therefore, is not exclusively a metal layer. The status of claims 1-4, 10-15, 17, and 18 should not change based on these amendments.

Claims 8 and 9 were objected to, but not rejected. The status of those claims should not change based on the amendment already described. No further comment is made as to those claims.

The rejection of claim 16 is moot in view of its cancellation.

Claims 5-7 were rejected as anticipated by the prior art described in the patent application with respect to Figures 6A and 14. This rejection is respectfully traversed as to amended claims 5-7.

Claim 5 has been amended to describe more specifically a metal interconnection layer and the location of the layer containing a metal. This amended claim is supported by the disclosure of the patent application with respect to the embodiments of Figures 7 and 12. In the embodiments of Figures 7 and 12, the first layer containing a metal corresponds to layer 124. In the embodiment of Figure 7, the signal interconnection layer of claim 6 corresponds to layers 108a and 109a. In the embodiment of Figures 7 and 12, the signal interconnection layer of claim 7 corresponds to the layer 126a. There is no layer similar to layer 124 in Figure 14 of the patent application and therefore the structure shown in that figure cannot anticipate amended claims 5-7.

Figure 6A of the patent application was relied upon for an entirely different element with respect to some of the claims. That figure does not suggest nor disclose the features of amended claim 5 that distinguish that claim from Figure 14 of the patent application. Therefore, the combination of those two figures cannot anticipate amended claims 5-7.

Claims 6-8 have been amended to conform to the amendment of claim 5. It is made clear in the amended claims that claims 6 and 7 refer to different layers from the first layer of claim 5 that extends from the DRAM region into the logic region.

New claims 19 and 20 are supported by the embodiment of Figure 12. The unnumbered layers corresponding to layers 108a and 109a of Figure 7 correspond to the second shielding layer of claim 19. These layers are common to the gate electrode layers 108 and 109, the reference numbers being provided in Figure 7 although not in Figure 12.

Reconsideration and allowance of all pending claims are earnestly solicited.

Respectfully submitted,

Jeffrey A. Wyand, Reg. No. 29,458
LEYDIG, VOIT & MAYER
700 Thirteenth Street, N.W., Suite 300
Washington, DC 20005-3960
(202) 737-6770 (telephone)
(202) 737-6776 (facsimile)

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